

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

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1. **(Previously Presented):** A fabrication method of a semiconductor device comprising the steps of:

forming a first insulation layer on a flat underlying face over a substrate,

introducing impurities into said first insulation layer, and

embedding and forming a first conductive layer in said first insulation layer by the

17 Damascene method.

2. **(Original):** The fabrication method of a semiconductor device according to claim 1, wherein said step of forming a first conductive layer includes the step of embedding the first conductive layer in said first insulation layer so as to expose a surface of said first conductive layer, and

said fabrication method further comprising the steps of:

forming a second insulation layer on said first insulation layer;

forming a contact hole in said second insulation layer, exposing a portion of said first conductive layer; and

forming a second conductive layer in said contact hole, electrically connected to said

first conductive layer.

3. **(Original):** The fabrication method of a semiconductor device according to claim 2, further comprising the step of introducing impurities into said second insulation layer.

4. **(Original):** The fabrication method of a semiconductor device according to claim 2, comprising, after formation of said second insulation layer and before formation of said contact hole, the steps of:

forming a first mask pattern on said second insulation layer;

forming a third insulation layer on said second insulation layer and on said first mask pattern,

forming a second mask pattern on said third insulation layer, having an opening larger than said first mask pattern, and

etching said third insulation layer using said second mask pattern to form a trench in said third insulation layer reaching to said first mask pattern,

wherein said step of forming a contact hole includes the step of etching said second insulation layer using said first mask pattern, and

wherein said step of forming a second conductive layer includes the step of forming a third conductive layer in said trench, electrically connected to said second conductive layer, in addition to formation of said second conductive layer.

5. **(Original):** The fabrication method of a semiconductor device according to claim 4, further comprising the step of introducing impurities into said third insulation layer.

6. **(Original):** The fabrication method of a semiconductor device according to claim 1, further comprising the step of forming a fourth insulation layer on said substrate prior to formation of said first insulation layer,

wherein said step of introducing impurities into the first insulation layer is carried out under a condition where introduced impurities arrive at an interface between said first insulation layer and said fourth insulation layer.

7. **(Original):** The fabrication method of a semiconductor device according to claim 1, wherein said first insulation layer includes a silicon oxide film containing at least 1% of carbon.

8. **(Original):** The fabrication method of a semiconductor device according to claim 2, wherein said second insulation layer includes a silicon oxide film containing at least 1% of carbon.

9. **(Original):** The fabrication method of a semiconductor device according to claim 4, wherein said third insulation layer includes a silicon oxide film containing at least 1% carbon.

10. **(Original)**: The fabrication method of a semiconductor device according to claim 1, wherein said first insulation layer includes an inorganic SOG film.

11. **(Previously Presented)**: The fabrication method of a semiconductor device according to claim 2, further comprising after formation of said second insulation layer and before formation of said contact hole, the steps of:

forming a mask pattern on said second insulation layer,

etching said second insulation layer using said mask pattern to selectively reduce thickness of said second insulation layer, and

forming another mask pattern on said second insulation layer so as to expose a portion of the region reduced in thickness,

wherein said step of forming a contact hole includes the step of etching said second insulation layer using said another mask pattern, and

said step of forming a second conductive layer includes the step of forming a third conductive layer on said region reduced in thickness, electrically connected to said second conductive layer, in addition to formation of said second conductive layer.

12. **(Original)**: The fabrication method of a semiconductor device according to claim 1, further comprising the steps of:

forming a second insulation layer on said first insulation layer,

forming a fifth mask pattern on said second insulation layer,  
etching said second insulation layer using said fifth mask pattern to form a contact hole in said second insulation layer, exposing a portion of said first conductive layer,  
after removing said fifth mask pattern, forming a resist film in said contact hole and on said second insulation layer,  
forming a sixth mask pattern on said contact hole, having an opening larger than that contact hole, by patterning said resist film on said second insulation layer,  
etching said second insulation layer using said sixth mask pattern to selectively reduce thickness of said second insulation layer,  
removing the resist film remaining in said contact hole and said sixth mask pattern,  
and  
forming a second conductive layer in said contact hole, electrically connected to said first conductive layer.

13. **(Original):** The fabrication method of a semiconductor device according to claim 2, further comprising the step of introducing impurities into said second insulation layer, prior to forming said contact hole in said second insulation layer.

14-20. **Canceled**

21. **(Currently Amended):** The fabrication method according to claim 1, wherein said first conductive layer is embedded only in said [trench] first insulation layer.

22. **(Previously Presented):** A fabrication method of a semiconductor device comprising the steps of:

forming a first insulation layer on a flat underlying face over a substrate,

introducing impurities into said first insulation layer,

forming a trench in said first insulation layer by etching,

embedding and forming a first conductive layer in said first insulation layer,

forming a second insulation layer on said flat first insulation layer and said flat first conductive layer,

introducing impurities into said second insulation layer,

forming a trench and a contact hole in said first insulation layer by etching,

embedding and forming a second conductive layer in said second insulation layer.

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